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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/224,756	01/04/1999	RICHARD PIERRE FOURNEL	S1022/8175	3287

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/224,756	FOURNEL, RICHARD PIERRE	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 and 3-12 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Miller.

In regards to claim 1, Miller shows all the elements of the claimed invention in figs. 1 and 2. It comprising a method for programming a read-only memory cell including a transistor [10] formed in a semiconductor substrate [12] of a first doping type (p-type), the transistor having a drain [20] and a source [18, (lightly doped n-type source region [26])] of a second doping type (n-type) separated in the substrate by a conduction channel [16, a top surface of p-type region [29]), the method comprising a step of: contradoping a first region of the source ([26] of fig. 1) such that the first region is of the first doping type ([26] of fig. 2 in transistor [32]) to prevent a transistor effect from occurring, the first region ([26] of fig. 2 in transistor [32]) directly contacting the conduction channel (the top surface of the p-type region [29]); wherein the step of contradoping includes a step of contradoping only the first region of the source of the transistor such that a second region of the source [18] remains of the second doping type.

In regards to claim 3, Miller shows all the elements of the claimed invention in figs. 1 and 2. It is a memory, in integrated circuit form, comprising: a plurality of transistors [30, 32] that form a corresponding plurality of memory cells, wherein each transistor has

a drain [20] and a source (18, n-type lightly doped source [26] of fig. 1) separated by a conduction channel (16, a top surface of each of the p-type regions [29]), wherein a first transistor [32] forms a corresponding programmed cell (a transistor that has a high threshold voltage), and wherein the conduction channel (the top surface of region [29]) and a first region of the source ([26] of fig. 2) of the first transistor [32] directly contact each other and wherein the first region is contradoped so that the first region (p-type region [26] of fig. 2 in transistor [32]) and the conduction channel (the top surface of region [29]) are of the same doping type (p-type), and wherein the drain [20] is not contradoped.

In regards to claim 4, Miller further discloses the drain [20] and a second region [18] of the source of the first transistor [32] are of the same doping type (n-type).

In regards to claim 12, Miller further discloses the first region ([26] of fig. 1) is originally of a doping type (n-type) that is opposite that of the conduction channel (the top surface of the p-type region [29] of fig. 1).

In regards to claim 5, Miller shows all the elements of the claimed invention in figs. 1 and 2. It is a memory, comprising: a plurality of cells [30, 32] formed in a substrate [12] of a first doping type (p-type), the plurality of cells including a first programmed cell [32] having a drain [20] of a second doping type (n-type), a conduction channel (16, a top surface of each of the p-type regions [29]) of the first doping type, a source (18, p-type lightly doped source [26] of fig. 2 in transistor [32]), wherein the source includes a first region [26] of the first doping type directly contacting the conduction channel (the top

surface of p-type region [29]); wherein the first region ([26] of fig. 2 in transistor [32]) is the only region in the source that is contradoped.

In regards to claim 6, Miller further discloses the source of the first programmed cell [32] further includes a second region [18] of the second doping type contacting the first region ([26] of fig. 2 in transistor [32]).

In regards to claim 7, Miller shows all the elements of the claimed invention in figs. 1 and 2. It is a memory, comprising: a plurality of cells [30, 32] formed in a substrate [12] of a first doping type (p-type), the plurality of cells including a first programmed cell [32] having a drain [20] of a second doping type (n-type), a conduction channel (16, a top surface of each of the p-type regions [29]) of the first doping type, and a source (18, p-type lightly doped source [26] of fig. 2 in transistor [32]) including non-conducting means ([26] of fig. 2 in transistor [32]) directly contacting the conduction channel (the top surface of the p-type region [29]) and being contradoped for providing a non-conducting response in the conduction channel to prevent a transistor effect from occurring between the drain and the source when predetermined voltages (the voltages below the high threshold voltage of transistor [32]) are applied to the first programmed cell to read the first programmed cell; wherein the non-conducting means ([26] of fig. 2 in transistor [32]) are the only region in the source that is contradoped.

In regards to claim 8, Miller further discloses the non-conducting means is a first region [26] of the source of the first programmed cell [32] contradoped such that the first region is of the first doping type to inherently form a degenerate transistor as the first programmed cell.

In regards to claim 9, Miller further discloses the first region of the source (p- region [26]) of the first programmed cell [32] has a doping concentration less than that of the n+ type drain [20].

In regards to claim 10, Miller shows all the elements of the claimed invention in figs. 1 and 2. It discloses a method for programming a cell [10], comprising the steps of: forming, in a substrate [12] of a first doping (p-type), a first transistor [10] having a drain [20] of a second doping type (n-type), and a source [18, (lightly doped n-type source region [26])] of the second doping type, such that a portion of the substrate forms a conduction channel ([16], a top surface of the p-type region [29]) between the source and the drain; and contradoping only a first region [26] of the source in the source region (fig. 2) which directly contacts the conduction channel to inherently make the first transistor degenerate.

In regards to claim 11, Miller further discloses the step of contradoping includes the step of dividing the source into the first region [26], and a second region [18].

3. Applicant's arguments filed 3/20/00 have been fully considered but they are not persuasive.

It is urged, in page 3 of the remarks, that Miller does not teach or suggest a method of programming a cell that includes a step of contradoping only a first region of the source as recited in claim 1. Since claim 1 never discloses a step of contradoping only a first region of the source in the entire transistor, it is possible to also contradoping the drain region or other region of the transistor. Therefore, Miller meets the limitation as claimed in claim 1.

It is urged, in pages 3-4 of the remarks, that the source of Miller is not directly contact the conduction channel [16]. However, as mentioned in the rejection, the source of Miller comprises both the n+ type region [18] and the lightly doped n-type source region [26] in the fig. 1. In addition, a top surface of the p-type region [29] and the p-type region [16] are considered as the channel of the transistor. Therefore, the n-type source region [26] (or the contradoped p-type source region [26]) is in direct contact with the conduction channel (the top surface of p-type region [29]).

It is urged, in page 4 of the remarks, that Miller fails to teach or suggest a source that includes a first region of a first doping type that directly contacting the conduction channel as recited in claim 5. However, as mentioned in the rejection, the source of Miller comprises both the n+ type region [18] and the lightly doped n-type source region [26] in the fig. 1. In addition, a top surface of the p-type region [29] and the p-type region [16] are considered as the channel of the transistor. Therefore, the contradoped p-type source region [26] (the first region of the first doping type) is in direct contact with the conduction channel (the top surface of p-type region [29]).

It is urged, in page 4 of the remarks, that Miller does not teach or suggest non-conducting means that are part of the source and directly contact the conduction channel. However, as mentioned in the rejection, the source of Miller comprises both the n+ type region [18] and the contradoped p-type source region [26] in fig. 2. In addition, a top surface of the p-type region [29] and the p-type region [16] are considered as the channel of the transistor. Therefore, the contradoped p-type source

region [26] is a part of the source and is in direct contact with the conduction channel (the top surface of p-type region [29]).

It is urged, in page 5 of the remarks, that Miller does not teach or suggest a step of contradoping only a first region of the source which directly contacts the conduction channel. Since claim 1 never discloses a step of contradoping only a first region of the source which directly contacts the conduction channel in the entire transistor, it is possible to also contradoping the drain region or other region of the transistor. Therefore, Miller meets the limitation as claimed in claim 10.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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October 27, 2004

Steven Loke
Primary Examiner